

HybriCore Chipset Product Brief

System Challenges

System architects and designers that are responsible for engineering the next generation of Enterprise Routers and Carrier Access equipment face some common challenges. Firstly, the emergence of new packet-based services are requiring systems to efficiently handle voice and video information, something that legacy architectures are not well suited for. High-bandwidth, multicast services such as IPTV place a particular strain on the systems that need to replicate and route that traffic. Secondly, there is the need to extend the useful life of a particular chassis development. For deployed systems, this requires strategies that enable the support of new services without the need for wholesale hardware replacements. New developments must be scalable to address emerging services. Finally, with few exceptions, the hardware aspect of these developments must be accomplished with smaller engineering teams inside ever-shrinking design cycles.

HybriCore Approach

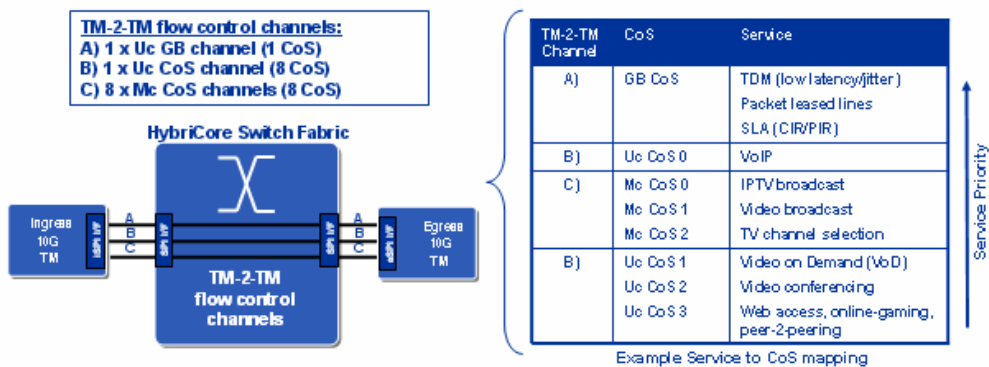
The HybriCore chipset from Enigma Semiconductor is designed to solve these challenges. This switching technology, which is optimized for use in chassis-based platforms, routes complete packets of any length across high speed serial links without any internal segmentation. The inclusion of a sophisticated scheduler ensures that packets are placed back-to-back. These factors combine to enable nearly 100% of the raw backplane serial link bandwidth to be allocated for handling real data (as opposed to packet tags). Compared with legacy switching architectures which need to run the serial links across the backplane at a higher speed (in some cases as much as 2x) to compensate for the inefficiencies of the switching, the use of the HybriCore chipset positively impacts system power, cost and reliability.

Enabling End-to-End QoS

Enigma's chipset is designed to address the challenges faced by designs of carrier class, multi-service platforms, including

- Migration of circuit based TDM services into a unified backplane
- Guaranteed delivery of a mix of business and residential services based on voice, video, and data
- Ability to offer and manage a range of different QoS services on per user basis
- Work conserving sharing of unused bandwidth to support statistical overbooking

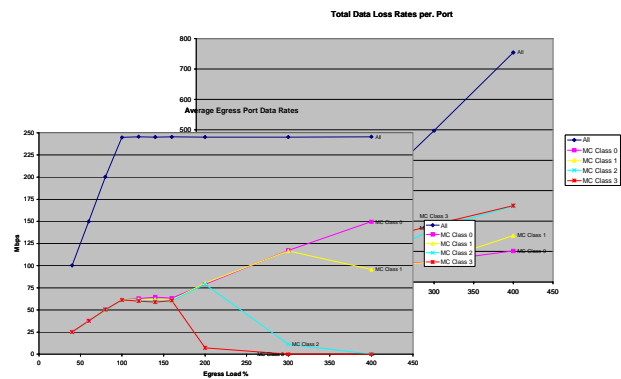
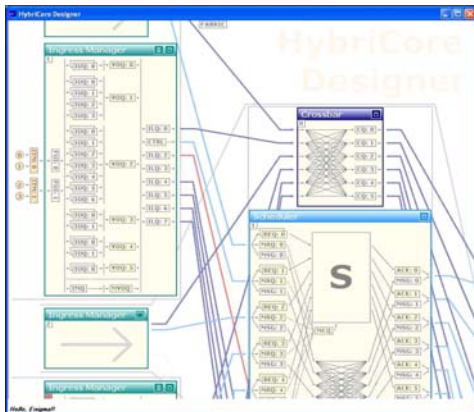
Enigma's chipset achieves its performance, power, PCB footprint and density leadership by relying on external traffic management devices. This model allows designers to select or design the appropriate traffic management (TM) device that aligns best to their requirements. It also allows designers to mix different types of TM devices inside a particular system and increases the flexibility of the system to support future services very efficiently.



Inside this type of system architecture, the TM device is used to manage per network port and per subscriber services. Network ports and subscribers are aggregated into TM to TM flow control channels across the switch. The number of flows and subscribers per TM can be scaled by utilizing new advanced TM devices, but the underlying switch fabric does not need to be modified. There are eight classes of service (CoS) that can be assigned per flow control channel. The chipset supports strict priority and/or deposit weighted round robin between the CoS. In many system examples, companies will offer guaranteed bandwidth services. However in periods when there is additional capacity across the network, there are opportunities for network operators to offer other revenue-generating services, by making this unused bandwidth available for other users. The TM device shares bandwidth between network ports and subscribers on a particular line card. The figure below provides an example as to how the HybriCore chipset could be configured to support a range of services.

For unicast traffic, the HybriCore chipset is a credits-based, pull architecture, with the traffic scheduling managed by the fabric manager device. Unicast traffic is prioritized ahead of multicast traffic. The chipset implements a two tier spatial replication process for multicast traffic in hardware, with the first tier handled by the switch device, and the second by the egress fabric manager.

Of course, each engineer is wrestling with a slightly different set of system requirements. Different data rates that need to be sustained, different profiles of traffic across those ports and a different set of services that the chassis must support. Enigma's modeling tool can be used to assist system architects make critical system decisions in the early phase of a development by configuring particular system topologies and traffic patterns and viewing the behavior of HybriCore chipset under these conditions.



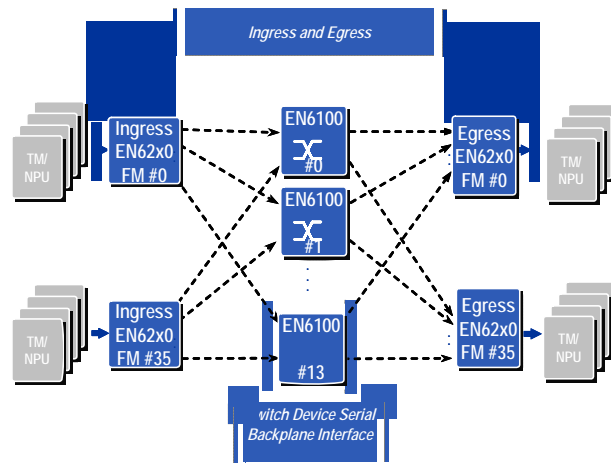
Delivering System Performance and Scalability

The chipset consists of two devices;

- The **Switch Device**, referred to by the EN6100 nomenclature, is a non-blocking, single-stage crossbar switch with 36 full duplex, high speed serial interfaces.
- The **Fabric Manager Device**, referred to by the EN6200 nomenclature, manages the flow of packets to and from the line card subsystem (network processor, dedicated traffic manager etc) and one or more switch devices, using full duplex high speed serial interfaces.

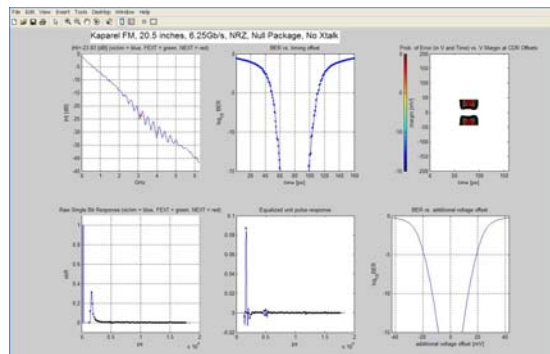
As figure x indicates, the first implementation of the HybriCore architecture can scale to support up to 36 line cards and 14 switch devices, which equates to an aggregate bandwidth of 2 Tbps.

Full duplex, high speed SERDES links are used to form the connection between the fabric manager (FM) and the switch device. These backplane serial links, shown in the dotted black lines in figure 1, are able to operate at **any** data rate between 2 Gbps and 12.5 Gbps, and support three CODEC options, NRZ, 64/66 and PAM4. Multi-tap equalization is employed in either signaling mode on both the transmitter and receiver for better signal integrity on the channel. The SERDES also incorporates on-chip active termination resistors, which precludes the need for external components and maximizes signal integrity.



With the larger switch device incorporating 36 such link pairs, the device can handle 360 Gbps of full duplex, non-blocking traffic. The family of FM devices include single chip 10 Gbps, 20 Gbps and 40 Gbps devices. The FM requires no external buffer memory, which significantly reduces the PCB footprint, power and cost of an Enigma-based line card implementation.

Enigma has developed a set of software tools that allow customers to predict the frequency improvement that the use of the HybriCore chipset will be able to deliver for a particular backplane. Enigma's simulation environment uses S-Parameter channel models. Unlike generic simulators, Enigma's simulator uses a behavioral model customized to the HybriCore chipset to accurately simulate its performance, by configuring link parameters such as data rate, the number of crosstalk aggressors, target BER, modulation type and encoding. Outputs from the tool provide numerical and graphical information that can be used to evaluate the amount of margin in the channel and channel performance.



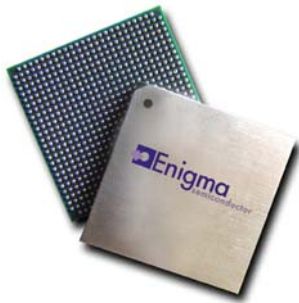
Product Family Summary

EN6200 Fabric Manager Family

Enigma Semiconductor currently offers three FM devices; a 10 Gbps device, a 20 Gbps device and a 40 Gbps device. These devices incorporate a SPI 4.2 interface(s) to connect to the line card subsystem and up to 14 serial links for connection to the switch. The differences between the devices are outlined in the table.

Attribute	EN6210	EN6220	EN6240	EN6240A
# of Serial Links	3	10	14	14
Effective Throughput (Gbps)	10	20	40	40
Max Serial Link Speed (Gbps)	6.25	6.25	10	12.5
Codecs Supported	2 (64/66, 8b/10b)	2 (64/66, 8b/10b)	3 (4PAM, 64/66, 8b/10b)	3 (4PAM, 64/66, 8b/10b)
# of SPI links	1	2	4	4
Package size / ball spacing (mm)	31x31 / 1	31x31 / 1	31x31 / 1	31x31 / 1
Maximum Power (W)	6	9	18	22

EN6100 Switch Family



The EN6100 switch device is a crossbar switch. It incorporates 36 serial links, all of which are capable of operating in the same 2.5 Gbps – 12.5 Gbps range as those on the FM components. This sets 36 as the maximum number of line cards that the initial instantiation of the HybriCore chipset can support. Up to 14 switches can be configured in parallel, to develop a chassis that is capable of supporting in excess of 2 Tbps. The family consists of two devices. One, the EN6105 device that incorporates 18 backplane serial links. The other, the EN6110 device, which includes 36 links.

Development Tools

Enigma has centered its reference board activities around an ATCA architecture, based on the availability of standard core components such as power supplies, chassis and backplanes, and the desire to align with reference boards initiatives from silicon partners developing NPU/TM devices.

In addition to the hardware platform, Enigma delivers a suite of software tools that are used to monitor and control the signal integrity (SI) characteristics of the backplane serial links.

